IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Confirmation No.: 4994

Jin MURAYAMA et al. Group Art Unit: 2622

Application No.: 09/892,506 Examiner: Gary Vieaux

Filed: June 28, 2001 Attorney Dkt. No.: 107317-00032

For: LINEAR IMAGE SENSOR CHIP AND LINEAR IMAGE SENSOR

DECLARATION UNDER 37 CFR §1.132

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

I, Jin Murayama, hereby declare and state:

1. I am one of the inventors of the subject matter of the above-identified application.

2. I am a citizen of Japan having a residence at 45-12 Yanagishinden, Odawara City, Kanagawa, Japan.

3. In March 1976, I graduated from Tokyo University, Faculty of Engineering, Division of Physical Engineering, and in March 1978, I graduated from master course of school of Engineering of Tokyo University, with a major in Physical Engineering.

4. From April 1978, I have worked for FUJIFILM Corporation, ex-FUJI PHOTO FILM CO., LTD. except for the period between April 1991 and March 2006, during which, I worked for FUJI FILM MICRODEVICES CO., LTD. From April 1978, I have been engaged with the research and development in solid state image pickup device.

5. I am a member of Japan Society of Applied Physics.

6. In the specification of the above-identified application, there is a description, "The bonding pads are formed along the peripheral area of the semiconductor substrate

either in the central area of the LIS semiconductor chip or in the opposite end areas along the longitudinal direction," in the "DESCRIPTION OF THE RELATED ART" at page 3, lines 8 – 10.

In Japanese Patent Application 2000-194500 filed on June 28, 2000, on which the above-identified application is based, the corresponding description is, "The bonding pads are formed along the peripheral edge areas of the semiconductor substrate either in the central area or in the opposite end areas along the longitudinal direction of the LIS semiconductor chip."

I intended to mean by this sentence that the LIS semiconductor chip (the semiconductor substrate) has the bonding pads along the peripheral edge areas, that the bonding pads may be formed along the peripheral edge areas in the central area, or may be formed along the peripheral edge areas in the opposite end areas, that a longitudinal central area is between the peripheral edge areas along the longitudinal direction, and that an image pickup section or a peripheral circuit section is formed in the longitudinal central area.

It was presumed that at least part of the bonding pads are located at the same longitudinal positions as the image pickup section or the peripheral circuit section.

I did not intend to mean by the above sentence that such a structure as that a plurality of bonding pads are formed on the surface of the semiconductor substrate in the opposite end areas not including the image pickup section nor the peripheral circuit section was prior art.

7. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that

these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that willful false statements may jeopardize the validity of the above-referenced application or any patent issuing thereon.

Jin Murayama Date: Nov. 16, 2006

Jin Murayama